

**REPLY UNDER 37 C.F.R § 1.116  
EXPEDITED PROCEDURE  
EXAMINING GROUP 3723**

**PATENT**  
5298-07600/PM01036

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:  
Zagrebelyn

§ Group Art Unit: 3723  
§ Examiner: Robert Rose  
§  
§ Atty. Dkt. No. 5298-07600

Serial No. 10/025,511

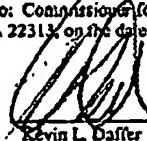
Filed: December 19, 2001

For: **METHODS FOR POLISHING A  
SEMICONDUCTOR TOPOGRAPHY**

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313, on the date indicated below:

September 30, 2004  
Date

  
Kevin L. Daffer

**SUPPLEMENTAL AMENDMENT; RESPONSE AFTER FINAL REJECTION  
PURSUANT TO 37 CFR § 1.116**

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313

Dear Sir/ Madam:

This paper is submitted in response to the final Office Action dated June 2, 2004 and the Advisory Action dated August 25, 2004 to further highlight reasons why the application is in condition for allowance.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims, which begins on page 4 of this paper.

Remarks begin on page 7 of this paper.